



# **Thunderbolt™ Release Notes For Tiger-Lake Integrated Thunderbolt (iTBT) A-Step**

**Release Notes - NDA**

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***January 2020***

***Revision 5.0***

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## ***Audience***

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This document intended for use by OEM software developers, test and validation engineers, and system integrators.



# Contents

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1	Introduction .....	6
	1.1 Scope of Document .....	6
	1.2 Acronyms .....	6
	1.3 Naming Convention .....	6
2	Features Supported .....	7
3	New Features—RCRs .....	8
4	Issue Status Definitions .....	9
	4.1 Fixed Issues in this Release .....	10
	4.2 Known Issues—To Date .....	11
	4.3 Archive—Fixes in Previous Releases .....	12



## Revision History

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Revision Number	Description	Revision Date
1.0	Initial release for iTBT A-Step	September 2019
2.0	Initial release for iTBT A-Step	November 2019
5.0	Initial release for iTBT A-Step	January 2020



# 1 Introduction

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## 1.1 Scope of Document

This document provides component-level details of the downloaded release and the contents of each folder in the release.

## 1.2 Acronyms

Term	Description
TBT	Thunderbolt™
HR	Host Router
EP	End-Point
AIC	Add-In Card
AR	Alpine Ridge (Thunderbolt™ 3)
TR	Titan Ridge (Thunderbolt™ 3)
GR	Goshen Ridge (Thunderbolt™ 4)
YFL	Yosemite Falls
ICL	Ice Lake
DP	Display Port
CM	Connection Manager
LC	Link Controller
HDCP	High-bandwidth Digital Content Protection
DB	Delta Bridge – TBT Retimer
P2P	Peer-to-Peer

## 1.3 Naming Convention

<project name>\_<Si stepping>\_<image rev>.bin

For example,  
<project name>:  
YFL, AR, TR, etc.

TGL\_A0\_Rev1.bin – Tiger Lake A0 stepping Revision 1



## 2 Features Supported

Supported = ✓ Limited Support = ⚠ Not Supported = ✗

Technology	Support
Thunderbolt Link 20/40G (Rounded)	✓
Thunderbolt Link 20.3/40.6G (Non-Rounded)	✓
Thunderbolt Link Power Management (CLx)	⚠
PCIe Tunnel	✓
DP Tunnel	✓
LTTPR	✓
DSC/FEC	✓
HDCP1.x	✓
HDCP2.x	✓
USB Tunnel	✓
USB Wake	✓
RTD3	✓
Wake from TBT	✗
SX	✓
P2P	✓



### 3 New Features—RCRs

RCR #	Title	Change Info	Status
<a href="#">1307111122</a>	Interdomain (Cross domain) sleep issue with S0ix	<b>Sighting #:</b> N/A <b>Affected Component:</b> LC <b>Impact:</b> Auto wake from S0ix if the link is inter-domain.	





## 4 *Issue Status Definitions*

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This document provides sightings and bugs report for Integrated Thunderbolt™ SKUs. At the time of a milestone release, this report will be distributed with the Intel® TBT Release and will provide information on new issues and the status of old issues (replacing the Release Notes document).

**Closed Issues:** This category will only display closed issues within the current Intel® TBT release. After each release, old issues will be dropped down to the "Archive" section and then new closed issues will take its place back up top for the next release. If an issue is posted in this section, it will indicate that the issue has been verified and fixed within the one that is being released.

**Known Issues:** This category will display all Known Issues since the initial release and will remain in this section until fixed or noted otherwise. "Known Issues" are still under investigation and may or may not be root caused.

**Archive – Fixes in Previous releases:** This category will display all closed issues that were closed in their respected release#. This section will serve as a history of fixed issues.

**Sightings listed in this document apply to the Integrated Thunderbolt™ SKUs unless noted otherwise in this document or in the sightings tracking systems.**



## 4.1 Fixed Issues in this Release

Issue Closed in Release #	Title	Details	Affected SKUs
5	<b>Blank Screen on Redriver Displays (DP/HDMI/VGA) when connected through TBT3 TR docks.</b>	<b>Sighting #:</b> <a href="#">1607953536</a> <b>Affected Component:</b> DP <b>Impact:</b> DP monitor doesn't work behind TR dock. <b>Fix:</b> dp_in will reply wrong EQ status (on first status read only) in order to get 16ms more for TMU convergence.	<b>All</b>



## 4.2 Known Issues—To Date

Issue Found in Release #	Title	Details	Affected SKUs
4	<b>ASUS TBT 3 Display detection failed with TBT integrated on all TCP ports</b>	<b>Sighting #:</b> <a href="#">16010689927</a> <b>Affected Component:</b> DP <b>Impact:</b> ASUS TBT 3 display doesn't detect on Type-C ports.	



## 4.3 Archive—Fixes in Previous Releases

Issue Fixed in Release #	Title	Details	Affected SKUs
4	5K TBT3 monitor fails after few hot-plugs	<p><b>Sighting #:</b> <a href="#">2209310272</a>  <b>Affected Component:</b> CM  <b>Impact:</b> After few hot plugs 5K TBT3 monitor fails to light up and there is no sign of the display in the display control panel in Windows, due to TBT not sending Resource Allocation and HPD to IOM.  <b>Fix:</b> Proper hop id allocation for DP ports on establishment of a DP tunnel and doing DP BW release on DP tear down now to cover all cases where CM need to release the BW.</p>	All
4	DP adapter resets with LTTTPR enabled each 5 sec in DP tunnel	<p><b>Sighting #:</b> <a href="#">1307052557</a>  <b>Affected Component:</b> DP  <b>Impact:</b> In DP tunnel with TR device, DP 1.4a monitor and LTTTPR enabled driver, DP FW doesn't raise valid bit which causes CM to tear down the path and DP_IN adapter to reset each ~5 sec.  <b>Fix:</b> In LTTTPR mode DP FW never read extended capabilities support reg 0xe because this transaction is external, the fix is always read 0x2200 extended capabilities.</p>	All
2	TBT LSx sideband clock is not correctly configured to 100 MHz	<p><b>Sighting #:</b> <a href="#">1306444014</a>  <b>Affected Component:</b> LC  <b>Impact:</b> TBT LSx sideband clock is not correctly configured to 100 MHz.  <b>Fix:</b> Changed tbt_car_cfg_uarttime_4 value to: 0xcb206464.</p>	All